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Term	Documents
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<u>L50</u>	l32 and l33	16	<u>L50</u>
<u>L49</u>	l32 and l38	3	<u>L49</u>
<u>L48</u>	l32 and l37	2	<u>L48</u>
<u>L47</u>	l32 and l35	0	<u>L47</u>
<u>L46</u>	l33 and l38	410	<u>L46</u>
<u>L45</u>	l33 and l37	835	<u>L45</u>
<u>L44</u>	l33 and l36	835	<u>L44</u>
<u>L43</u>	l33 and l35	71	<u>L43</u>
<u>L42</u>	(712/227,228)[CCLS]	1199	<u>L42</u>
<u>L41</u>	(712/228)[CCLS]	597	<u>L41</u>
<u>L40</u>	(718/102-108)[CCLS]	4064	<u>L40</u>

<u>L39</u>	(718/102-108)![CCLS]	4064	<u>L39</u>
<u>L38</u>	(718/102-108)[CCLS]	4064	<u>L38</u>
<u>L37</u>	(712/219,245)[CCLS]	835	<u>L37</u>
<u>L36</u>	(712/219,245)![CCLS]	835	<u>L36</u>
<u>L35</u>	(713/375,401)[CCLS]	829	<u>L35</u>
<u>L34</u>	(712/2-300)[CCLS]	12305	<u>L34</u>
<u>L33</u>	(712/2-300)![CCLS]	12305	<u>L33</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L32</u>	(stipulat\$5 or schedul\$4 of DEFAULT) near12 (halt\$5 or stop\$5 or suspend\$5 or held or hold\$3 or disabl\$5) near15 pipelin\$4	54	<u>L32</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L31</u>	L30 and (allocat\$6 or assign\$7 or DEFAULT OR schedul\$4 OR FORC\$4)	1	<u>L31</u>
<u>L30</u>	6216232.pn.	1	<u>L30</u>
<u>L29</u>	L24 and (allocat\$6 or assign\$7 or DEFAULT OR schedul\$4 OR FORC\$4)	0	<u>L29</u>
<u>L28</u>	L24 and (assign\$7 or DEFAULT OR schedul\$4 OR FORC\$4)	0	<u>L28</u>
<u>L27</u>	L24 and (DEFAULT OR schedul\$4 OR FORC\$4)	0	<u>L27</u>
<u>L26</u>	L24 and schedul\$4	0	<u>L26</u>
<u>L25</u>	L24 and schedul\$	0	<u>L25</u>
<u>L24</u>	6609193.pn.	1	<u>L24</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L23</u>	L19 and 19	0	<u>L23</u>
<u>L22</u>	L19 and 18	3	<u>L22</u>
<u>L21</u>	L19 and 17	4	<u>L21</u>
<u>L20</u>	L19 and 16	15	<u>L20</u>
<u>L19</u>	15 and general near2 purpose	63	<u>L19</u>
<u>L18</u>	15 and general near21 purpose	63	<u>L18</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L17</u>	13 and 19	4	<u>L17</u>
<u>L16</u>	13 and 18	6	<u>L16</u>
<u>L15</u>	13 and 17	5	<u>L15</u>
<u>L14</u>	13 and 16	21	<u>L14</u>
<u>L13</u>	12 and 19	7	<u>L13</u>
<u>L12</u>	12 and 18	9	<u>L12</u>
<u>L11</u>	12 and 17	7	<u>L11</u>
<u>L10</u>	12 and 16	35	<u>L10</u>
<u>L9</u>	(710/60-68)[CCLS]	2714	<u>L9</u>
<u>L8</u>	(712/225,227,300)[CCLS]	1502	<u>L8</u>
<u>L7</u>	(712/4-22)[CCLS]	1719	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	12305	<u>L6</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L5</u>	L3 and vector\$1	79	<u>L5</u>
<u>L4</u>	L3 and (simd or single near1 instruction near3 data)	7	<u>L4</u>

<u>L3</u>	L1 near15 (instruction\$1 or command\$3 or micro near2 instruction\$1) near10 (field\$1 or portion\$1 or portion\$1 or section\$1 or but\$1 or byte\$1)	272	<u>L3</u>
<u>L2</u>	L1 near15 (instruction\$1 or command\$3 or micro near2 instruction\$1) (number) near15 (indicat\$4 or specif\$6) near15 (transfer\$6 or sent or	425	<u>L2</u>
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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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Manne, S.; Klauser, A.; Grunwald, D.;
[Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on](#)
27 June-1 July 1998 Page(s):132 - 141
Digital Object Identifier 10.1109/ISCA.1998.694769
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- ☐ 2. **An efficient pipelined dataflow processor architecture**
Dennis, J.B.; Gao, G.R.;
[Supercomputing '88. \[Vol. 1\]. Proceedings.](#)
14-18 Nov. 1988 Page(s):368 - 373
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- ☐ 3. **Implementing register interlocks in parallel-pipeline, multiple instruction queue, superscalar**
Weiss, S.;
[High-Performance Computer Architecture, 1995. Proceedings. First IEEE Symposium on](#)
22-25 Jan. 1995 Page(s):14 - 21
Digital Object Identifier 10.1109/HPCA.1995.386559
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- ☐ 4. **A methodology for evaluating the performance of RISC processors**
Obaidat, M.S.; Abu-Saymeh, D.S.;
[Applied Computing, 1991. \[Proceedings of the 1991 Symposium on\]](#)
3-5 April 1991 Page(s):213 - 222
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- ☐ 5. **A result forwarding mechanism for asynchronous pipelined systems**
Gilbert, D.A.; Garside, J.D.;
[Advanced Research in Asynchronous Circuits and Systems, 1997. Proceedings. Third International](#)
7-10 April 1997 Page(s):2 - 11
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Iacobovici, S.; Iacobelli, F.;

[VLSI Technology, Systems and Applications, 1989. Proceedings of Technical Papers, 1989. Internat](#)
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Oklobdzija, V.G.;

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8. Use-based register caching with decoupled indexing

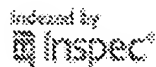
Butts, J.A.; Sohi, G.S.;

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